Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A process ~~for~~used in fabricating a liquid crystal display, comprising the steps of:

a) preparing a substrate having a major surface;

b) patterning a first conductive material layer into plural gate layers and plural storage electrode layers on said major surface;

c) covering said plural gate layers and said plural storage electrode layers with a gate insulating layer;

d) patterning an amorphous silicon layer into plural amorphous silicon layers on said gate insulating layer;

e) selectively etching said gate insulating layer together with ~~a piece~~pieces of residual amorphous silicon to form plural bent contact slits in said gate insulating layer; ~~connected between two of said plural amorphous silicon layers, for forming contact slits in said gate insulating layer, a piece of conductive material between one of said plural gate layers and an adjacent storage electrode layer being exposed to one of said contact slits, if any;~~

f) patterning a second conductive material layer into plural drain layers and plural source layers~~, said piece of conductive material being split during the pattering of said second conductive material layer~~; and

g) patterning a transparent material layer into pixel electrodes respectively held in contact with said plural source layers; ~~and~~

~~h) completing said liquid crystal display.~~

wherein a first bent contact slit of said plural bent contact slits is formed by etching said gate insulating layer together with pieces of said residual amorphous silicon from a top portion of said gate insulating layer through said gate insulating layer to said major surface of said substrate between a first gate layer of said plural gate layers and a first area where a first drain layer of said plural drain layers adjacent to said first gate layer is patterned, and by

etching said gate insulating layer together with pieces of said residual amorphous silicon from said top portion of said gate insulating layer through said gate insulating layer to said major surface of said substrate between said first area where said first drain layer is patterned and a first storage electrode layer of said plural storage electrode layers adjacent to said first area.

2. (Cancelled)